A32B Datesheet

Althico

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Revision History

修订日期	版本	修订内容
2021年5月31日	0.0.1	初稿
2021年8月2日	1.0.0	增加封装尺寸图

编码说明：

Bit 1 – 3 4 5-7 8-9

A32 B Q76 DC

1~3 位 ：A32 四位处理器型号
4 位 ：MCU 序列
5~7 位 ：QFN76
8~9 位 ：特性

Production / Parameter	A32BQ7DC
Ram	64KB
Flash	512KB
NFC	NA
ICC	2 Group
Tamper	4 Group Dynamic
ADC (3 group MSR)	8pin
Pin	76
GPIO	39
Authority Zone	Global
Release status	Yes

Introduction

A32BQ76xx is a multi-purpose MCU. The temperature range is of -25 to 85.
The operating frequency is 80MHz.
Chip package is:

- QFN76

Features

– 32-bit load/store reduced instruction set computer (RISC) architecture
with fixed 16-bit instruction length
– 16 entry 32-bit general-purpose register file
– Support for byte/halfword/word memory accesses
– Embedded interrupt controller, support nested vector interrupts.

• Cache
– Has two AHB bus interfaces, a master and a slave interface.
– Has a 2-way set-associative organization.
– Uses both the positive and negative edges of its single clock input
– Has an AHB bus interface to access its programmer's model.

OnCE debug support

• 64K Bytes of static random-access memory (SRAM):
– Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes

• 512K Bytes embedded flash (EFLASH)
– 512 Bytes page size

– Read Access Time:
50ns(max) @ EV=PV=0
200ns(max)@EV=1 or PV=1
– Endurance : 100000 Cycles(Min)
– Greater than 10 years under room temperature
– Fast Page Erase/Word Program
– Program Time of each pulse : 4.4us(Max)
– Program hold time:20ns(min)
– Mass Erase Time : 40ms(Max)
– Single cycle byte, half-word(16-bits) and word(32-bits) read access

• CPM
– Two system clock sources
Internal high speed 160MHz oscillator
Internal low speed 1MHz oscillator
– Separate clock divider
– Support for power saving mode

– Module clock can be gated separately
• Two Periodic interval timer :
– 16-bit counter with modulus "initial count" register
– Selectable as free running or count down

• Watchdog timer :
– 16-bit counter with modulus "initial count" register
– Pause option for low-power modes
• Time Counter :
– 16-bit counter with modulus "initial count" register
– Pause option for low-power modes

• Reset :
– Separate reset in and reset out signals
– Five sources of reset:
Power-on reset
Software reset
Watchdog timer
Real Time Counter
Power Attack Detect Reset (Low and High Voltage Detect Reset)
– Status flag indicates source of last reset

• DMA Controller
– Six independently programmable DMA controller channels
– Data transfers in 8, 16, 32 ,64bits
– Support single transfer, Burst 4, 8,16 transfer, and burst always under a speical case.
– Support single cycle transfer
– Support automatic transfer mode
– Support LLI transfer mode
– Follow a fixed priority rule

• External interrupts supported(EPORT) :
– Rising/falling edge select
– Low-level sensitive
– Ability for software generation of external interrupt event
– Interrupt pins configurable as general-purpose I/O

• I2C Controller
– Supports 7 bit addressing.
– Supports Standard Mode, Fast Mode and High-Speed Mode
– Software option to select between High-Speed mode and Standard/Fast mode
– Compatibility with standard and fast-mode of I2C bus version 2.1

standard.
– Multiple-master operation.
– Software-programmable for one of 64 different serial clock frequencies.
– Software-selectable acknowledge bit.
– Interrupt-driven, byte-by-byte data transfer.
– Arbitration-lost interrupt with automatic mode switching from master to slave.
– Transfer completion and read configure interrupt.
– Start and stop signal generation/detection.
– Repeated START signal generation.
– Acknowledge bit generation/detection.
– Bus-busy detection.
– Option slave address receiving enable when system clock stop mode
– SCL or SDA line gpio function supported

• Serial communications interface (SCI-UART):
– Full-duplex operation
– 13-bit baud rate prescaler
– Programmable 8-bit or 9-bit data format
– Separately enabled transmitter and receiver
– Separate receiver and transmitter CPU interrupt requests
– Two receiver wakeup methods (idle line and address mark)
– Receiver framing error detection
– Hardware parity checking
– 1/16 bit-time noise detection
– General-purpose I/O capability

• Memory Integration Module:
– Two Chip Select channel, two for external SRAM,NORFLASH and memory mapped peripherals(Only for evaluation)
– Support for swap and bootload modes
– Bidirectional data bus with wide 16-bit and narrow 8-bit modes
– 20-bits address bus
– Bus monitor

• Serial peripheral interfaces (SPI) :
– Master mode and slave mode configurable
– Slave select output
– Mode fault error flag with CPU interrupt capability
– Double-buffered receiver
– Serial clock with programmable polarity and phase
– Control of SPI operation during wait mode

• USB

– Supports internal reference clock or external 12MHz crystal reference clock
– Compliant with USB 1.1 specification with on-chip integrated PHY module
– Supports FS (12Mbps) modes
– Supports eight transmit/receive endpoints(ep0,ep1,ep2,ep3,ep4,ep5,ep6,ep7)

• PWM
– Programmable period
– Programmable duty cycle
– Two Dead-Zone generator
– Capture function
– Pins can be configured as general-purpose I/O

• ADC
– 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
– ADC conversion time: 1.0 ms for 12-bit resolution (1 MHz), 0.88 ms conversion time for 10 bit resolution, faster conversion times can be obtained by lowering resolution.
– Programmable sampling time
– DMA support

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• TRNG(random number generator)
– Rate: 250kbps

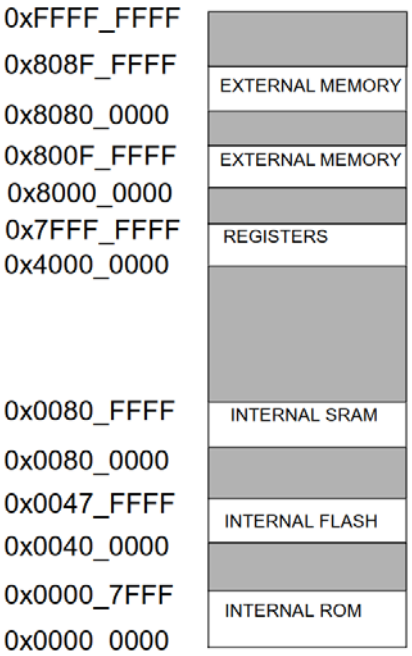
• PMU_RTC
– Load time data to and read time data from seconds, minutes, hours and days counters
– Support alarm settings
– Interrupt sources:second, minute, hour,day interrupts,programmable alarm interrupts ,1KHZ/32KHZ periodic interrupts .

Introduction

The address map, shown in **2.2**, includes:

- 64K Bytes of internal static random-access memory (SRAM)
- 512K Bytes Embedded Flash

• Internal memory mapped registers

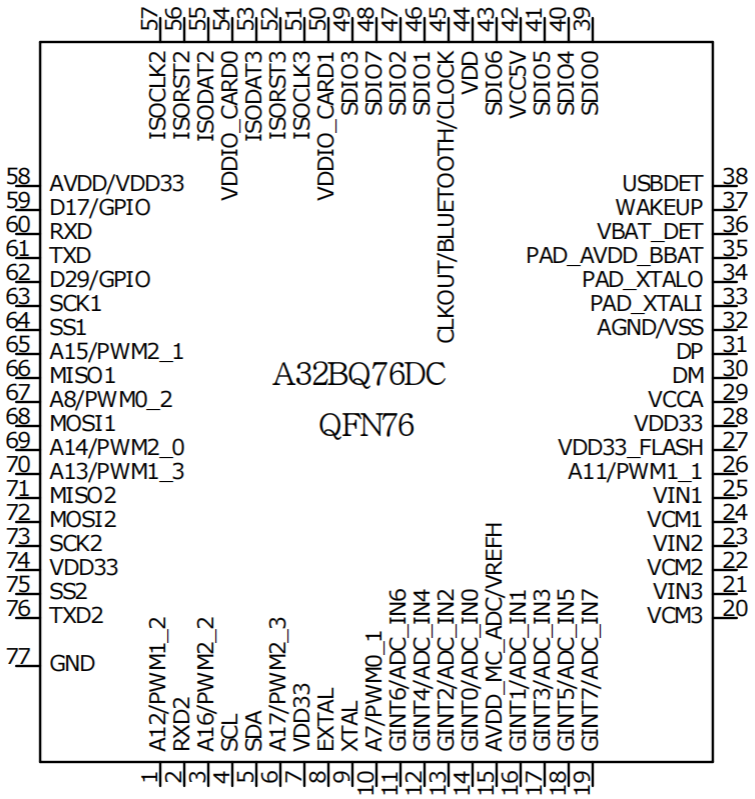


Pin Description

This section contains both a package pinout and tabular listings of the signal descriptions.The following nomenclature is used for Signal types:

GND	A Ground Signal
IA	Analog input signal
I	Digital input signal
IH	Input signals with weak internal pull-up, to prevent signals fromfloating when left open
IL	Input signals with weak internal pull-down, to prevent signals from floating when left open
I/O	A digital bi-directional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

Pin Assignments(QFN76)



Signal-to-Pin Relationships and Descriptions

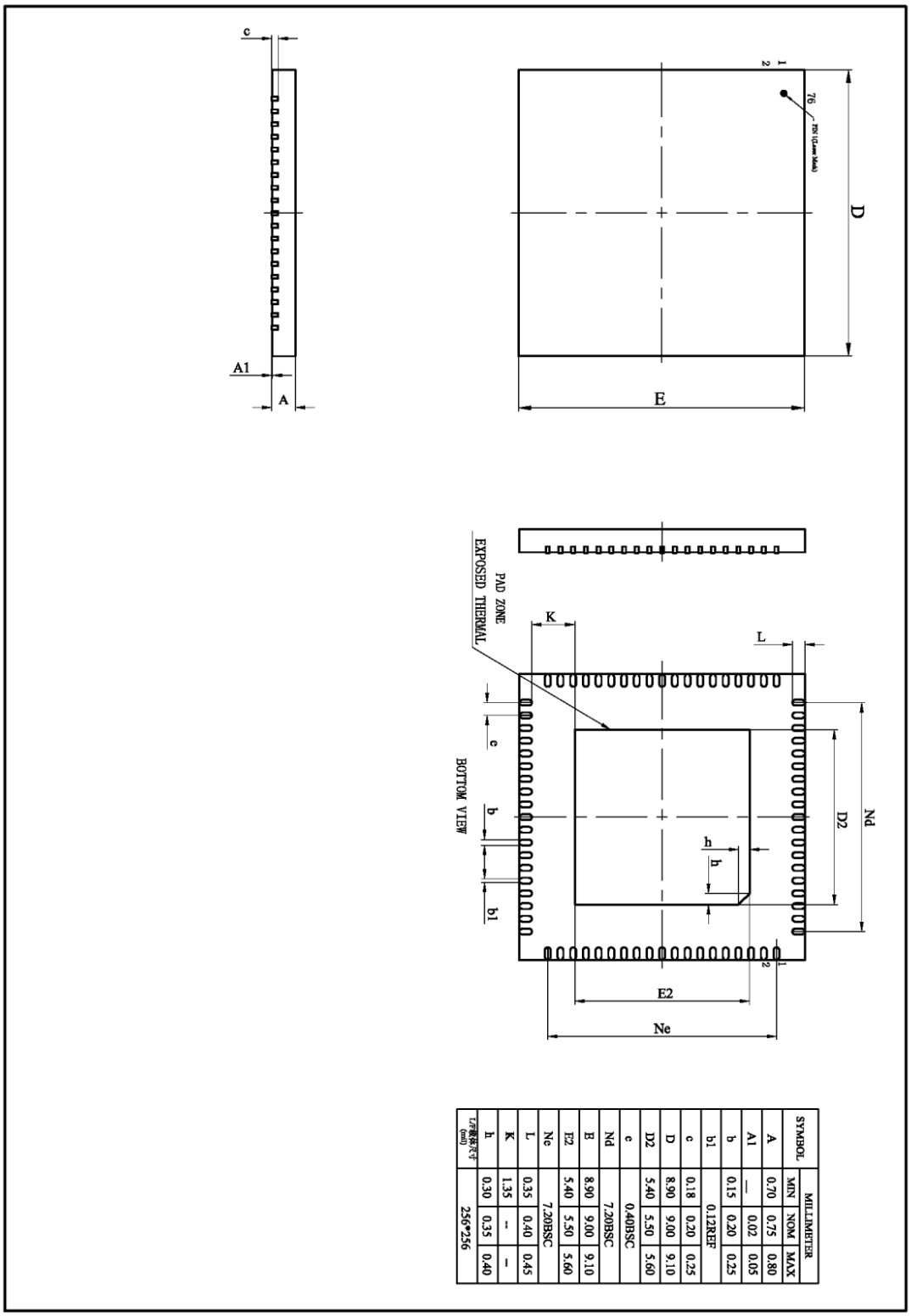
Name1	Alternate	Dir.	Pull	Voltage	Function
Serial Periheral Interface(SPI1/2)(8)					
mosi1	GPIO	I/O	Pullup	3.3v	Serial data output from the SPI in master mode and the serial data input in slave mode.
miso1	GPIO	I/O	Pullup	3.3v	Serial data input to the SPI in master mode and the serial data output in slave mode.
sck1	GPIO	I/O	Pullup	3.3v	The serial clock synchronizes data transmissions between master and slave devices. SCK is an output if the SPI is configured as a master. sck1 is an input if the SPI is configured as a slave.
ss1	GPIO	I/O	Pullup	3.3v	Peripheral chip select signal in master mode and is an active-low slave select in slave mode.
mosi2	GPIO	I/O	Pullup	3.3v	Serial data output from the SPI in master mode and the serial data input in slave mode.
miso2	GPIO	I/O	Pullup	3.3v	Serial data input to the SPI in master mode and the serial data output in slave mode.
sck2	GPIO	I/O	Pullup	3.3v	The serial clock synchronizes data transmissions between master and slave devices. SCK is an output if the SPI is configured as a master. sck1 is an input if the SPI is configured as a slave.
ss2	GPIO	I/O	Pullup	3.3v	Peripheral chip select signal in master mode and is an active-low slave select in slave mode.
I2C Interface(2)					
scl	GPIO	I/O	Pullup	3.3v	I2C controller bidirection clock pin..
sda	GPIO	I/O	Pullup	3.3v	I2C controller bidirection data pin.
GPIO(2)					
d[17]	GPIO	I/O	Pullup	3.3v	GPIO
d[29]	GPIO	I/O	Pullup	3.3v	GPIO
Edge Port (EPORT) (8)					
gint[0]/adc_in[0]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[1]/adc_in[1]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[2]/adc_in[2]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[3]/adc_in[3]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[4]/adc_in[4]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.

gint[5]/adc_in[5]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[6]/adc_in[6]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
gint[7]/adc_in[7]	GPIO	I/O	Pullup	3.3v	External interrupt source or GPIO. ADC analog channels.
USB2.0(2)					
dp	-	I/O	-	5v	USB D+ signal pin.
dm	-	I/O	-	5v	USB D- signal pin.
MCC(6)					
VIN1	-	I	-	3.3v	Magnet card reader channel 1 pad. Vin 1 is positive port.
VCM1	-	O	-	3.3v	Magnet card reader channel 1 pad. Vcm1 is negtive port.
VIN2	-	I	-	3.3v	Magnet card reader channel 2 pad. Vin 2 is positive port.
VCM2	-	O	-	3.3v	Magnet card reader channel 2 pad. Vcm2 is negtive port.
VIN3	-	I	-	3.3v	Magnet card reader channel 3 pad. Vin 3 is positive port.
VCM3	-	O	-	3.3v	Magnet card reader channel 3 pad. Vcm3 is negtive port.
SCI--UART(4)					
txd	-	I/O	Pullup	3.3v	SCI transmitter data output or GPIO
rxd	-	I/O	Pullup	3.3v	SCI receiver data input or GPIO
txd2	-	I/O	Pullup	3.3v	SCI transmitter data output or GPIO
rxd2	-	I/O	Pullup	3.3v	SCI receiver data input or GPIO
Other type pins(2)					
usbdet	-	I	-	5v	usb wake up detect pin. is 1 will wake up system when system enter powerdown mode.
WAKEUP	-	I	-	5v	External wake up signal. is1 will wake up system when system enter powerdown mode.
ISO-7816 Interface (USI2) (6)					
isoclk2	GPIO	I/O	-	1.8/3	Smart Card clock signal.
isodat2	GPIO	I/O	-	1.8/3	Smart Card Interface data input/output
isorst2	GPIO	I/O	-	1.8/3	Smart Card reset signal.
Isoclk3	GPIO	I/O	-	1.8/3	Smart Card clock signal.
Isodat3	GPIO	I/O	-	1.8/3	Smart Card Interface data input/output
Isorst3	GPIO	I/O	-	1.8/3	Smart Card reset signal.
PWM(9)					

a[8]/PWM0_2	GPIO	I/O	-	3.3v	pwm0[2] data input/output signal.
a[13]/PWM1_3	GPIO	I/O	-	3.3v	pwm1[3] data input/output signal.
a[14]/PWM2_0	GPIO	I/O	-	3.3v	pwm2[0] data input/output signal.
a[15]/PWM2_1	GPIO	I/O	-	3.3v	pwm2[1] data input/output signal.
a[12]/PWM1_2	GPIO	I/O	-	3.3v	pwm1[2] data input/output signal.
a[16]/PWM2_2	GPIO	I/O	-	3.3v	pwm2[2] data input/output signal.
a[17]/PWM2_3	GPIO	I/O	-	3.3v	pwm2[3] data input/output signal.
a[7]/PWM0_1	GPIO	I/O	-	3.3v	pwm0[1] data input/output signal.
a[11]/PWM1_1	GPIO	I/O	-	3.3v	pwm1[1] data input/output signal.
SDI(8)					
SDI0	-	I/O	-	5v	Self-destruction detect input.
SDI1	-	I/O	-	5v	Self-destruction detect input.
SDI2	-	I/O	-	5v	Self-destruction detect input.
SDI3	-	I/O	-	5v	Self-destruction detect input.
SDI4	-	I/O	-	5v	Self-destruction detect input.
SDI5	-	I/O	-	5v	Self-destruction detect input.
SDI6	-	I/O	-	5v	Self-destruction detect input.
SDI7	-	I/O	-	5v	Self-destruction detect input.
Power Supply(10)					
VDD33	-	-	-	-	This signal supplies 3.3V positive power output.
AVDD_MC_ADC /VREFH	-	-	-	-	ADC power supply,3.3v
VDD33_FLASH	-	-	-	-	This signal is the power supply for external flash.
VCCA	-	-	-	-	This signal is the 3.3v power supply for USB analog model.
PAD_AVDD_BBAT	-	-	-	-	RTC battery power supply.
VBAT_DET	-	-	-	-	5V battery power detect pad.
VCC5V	-	-	-	-	5v power supply
VDD	-	-	-	-	1.2v Power output
VDDIO_CARD0	-	-	-	-	Power supply for ISO7816 card.
VDDIO_CARD1	-	-	-	-	Power supply for ISO7816 card.
Clock(5)					
PAD_XTALI	-	I	-	3.3v	32.768KHz Oscillator input.
PAD_XTALO	-	0	-	3.3v	32.768KHz Oscillator output.
extal	-	I	-	3.3v	12MHz Oscillator input.
xtal	-	0	-	3.3v	12MHz Oscillator output
clkout	-	0	-	5v	Internal clock output

封装尺寸

单位：mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
b1		0.12REF	
c	0.18	0.20	0.25
D	8.90	9.00	9.10
D2	5.40	5.50	5.60
e		0.40BSC	
Nd		7.20BSC	
E	8.90	9.00	9.10
E2	5.40	5.50	5.60
Ne		7.20BSC	
L	0.35	0.40	0.45
K	1.35	--	--
h	0.30	0.35	0.40
LFBGA尺寸 (mil)	256*256		