A32DQ169
E1

DataSheet

Rev1.0

www.althico.com

Revision History

Release Number	Date	Author	Summary of Changes
1.0	2021/08/09	althico	This version is for initial version

Section 1 Introduction

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Section 1 Introduction

1.1 Introduction

A32DQ169E1 is a multi-purpose MCU based on the Cortex-M4F central processor unit (CPU).

The temperature range is of -25^{O}C to 85^{O}C.The operating frequency is up to 500MHz at typical condition.

Chip package is:

- BGA169

1.2 Features

Features of A32DQ169E1:

- Cache
  - Has two AHB bus interfaces, a master and a slave interface.
  - Has a 2-way set-associative organization.
  - Has an AHB bus interface to access its programmer's model.
- OnCE debug support
- On-chip, 64K Bytes of static random-access memory can only be accessed by CPU(TCMSRAM)
- On-chip, 128K Bytes of static random-access memory (SRAM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) reads and writes
- On-chip, 64K Bytes of static read only memory (ROM):
  - Single cycle byte, half-word (16-bit), and word (32-bit) read access.
- On-chip embedded flash (EFLASH)

  - Memory Origanization: 256K Bytes LP
  - Read of bytes, aligned halfwords (16 bits) and aligned words (32 bits)
  - Automated program and erase operation
  - Optional interrupt on command completion
  - Data Retention: 10 years under 85 degrees
  - 0.99~1.21V/1.5~1.98V dual power supplies
- CPM
  - Multiple system clock sources
  - Separate clock divider
  - Support for power saving mode
  - Module clock can be gated separately
- Programmable 32bit Interrupt timer(PIT) :
  - 32-bit counter with modulus "initial count" register
  - Selectable as free running or count down
  - 32 selectable prescalers — 2^0 to 2^{31}
- Watchdog timer(WDT) :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Time Counter :
  - 16-bit counter with modulus "initial count" register
  - Pause option for low-power modes
- Reset :
  - Separate reset in and reset out signals
  - Five sources of reset:
    Power-on reset
    Software reset
    Watchdog timer
    Time Counter
    Power Attack Detect Reset (Low and High Voltage Detect Reset)
  - Status flag indicates source of last reset

- DMA Controller
  - Four independently programmable DMA controller channels
  - Data transfers in 8, 16, 32 bits
  - Support single transfer, Burst 4, 8,16 transfer, and burst always under a speical case.
  - Support single cycle transfer
  - Support automatic transfer mode
  - Support LLI transfer mode
  - Follow a fixed priority rule
- EDMAC
  - Programmable transfer total number
  - Programmable read buffer address and write buffer address
  - Support read, write and write then read transfer
- CRC coprocessor
  - Support CRC32 / CRC16 / CRC8
  - Support DMAC Data from CRC
  - Support EDMAC Data from CRC
- External interrupts supported(EPORT):
  - Rising/falling edge select
  - Low-level sensitive
  - Ability for software generation of external interrupt event
  - Interrupt pins configurable as general-purpose I/O
- I2C Controller
  - Supports 10 bit addressing.
  - Supports Standard Mode, Fast Mode and High-Speed Mode
  - Software option to select between High-Speed mode and Standard/Fast mode
  - Compatibility with standard and fast-mode of I2C bus version2.1 standard.
  - Multiple-master operation.
  - Software-programmable for one of 64 different serial clock frequencies.

  - Software-selectable acknowledge bit.
  - Interrupt-driven, byte-by-byte data transfer.
  - Arbitration-lost interrupt with automatic mode switching from master to slave.
  - Transfer completion and read configure interrupt.
  - Start and stop signal generation/detection.
  - Repeated START signal generation.
  - Acknowledge bit generation/detection.
  - Bus-busy detection.
  - Option slave address receiving enable when system clock stop mode
  - SCL or SDA line gpio function supported
- Serial communications interface (SCI_BT):
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format
  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial communications interface (SCI):
  - Separate 16x9 transmit (TX) and receive (RX) FIFOs to reduce CPU interrupt service loading
  - FIFO trigger levels of 1/8, 1/4, 1/2, 3/4, and 7/8
  - Automatic hardware flow control supported
  - Serial IR interface low-speed,IrDA-compatible(up to 115.2Kbit/s)
  - Full-duplex operation
  - 13-bit baud rate prescaler
  - Programmable 8-bit or 9-bit data format

  - Separately enabled transmitter and receiver
  - Separate receiver and transmitter CPU interrupt requests
  - Two receiver wakeup methods (idle line and address mark)
  - Receiver framing error detection
  - Hardware parity checking
  - 1/16 bit-time noise detection
  - General-purpose I/O capability
- Serial peripheral interfaces (SPI) :
  - Master mode and slave mode configurable
  - Slave select output
  - Mode fault error flag with CPU interrupt capability
  - Separate transmit and receive FIFOs
  - Serial clock with programmable polarity and phase
  - Control of SPI operation during doze mode
- Inter-IC sound interfaces (I2S) :
  - Half-duplex communication
  - Master operations
  - Programmable prescaler to reach accurate audio sample frequencies
  - 16-bit Data format
  - Packet frame is fixed to 16-bit by audio channel
  - Underrun/overrun flag in transmission mode, overrun flag in reception mode
  - Supported I2S Philips standard protocols
  - Data direction is always MSB first
- USBOTG1.1
  - Supports internal reference clock or external 12MHz crystal reference clock
  - Performs all transaction scheduling in hardware
  - Operates either as a function controller for a USB peripheral or as the host/peripheral in point-to-point communications with another USB function
  - Synchronous RAM interface for FIFOs
  - Supports point-to-point communications with one full-speed device

- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
- Supports Suspend and Resume
- Configurable for up to 15 additional Transmit endpoints and up to 15 additional Receive endpoints
- Configurable FIFOs, including the option of dynamic FIFO sizing

  - Support for DMA access to FIFOs
- Soft connect/disconnect optionPWM
  - Programmable period
  - Programmable duty cycle
  - Two Dead-Zone generator
  - Capture function
  - Pins can be configured as general-purpose I/O
- PWMT
  - 16-bit up, down, up/down auto-reload counter
  - 16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536
  - Up to 4 independent channels
  - Complementary outputs with programmable dead-time
  - Synchronization circuit to control the timer with external signals and to interconnect several timers together
  - Repetition counter to update the timer registers only after a given number of cycles of the counter
  - Interrupt/DMA generation on the some events
- Controller Area Network (CAN):
  - Full implementation of the CAN protocol specification, version 2.0B
  - Flexible Message Buffers (up to 64) of zero to eight bytes data length
  - Programmable loop-back mode supporting self-test operation
  - Time Stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Ethernet MAC:
  - Compliant with RMII
  - Include internal DMA
  - Include RXFIFO and TXFIFO
  - Maskable interrupts
  - Automatic receiving data according to the actual length of the frame

- SD_HOST 2.0:
  - Supports Secure Digital I/O protocol commands
  - Supports Command Completion signal and interrupt to host processor
  - Single-channel; single engine used for Transmit and Receive, which are mutually exclusive
  - Fully synchronous design operating on a single system clock
  - Dual-buffer and chained descriptor linked list
  - Programmable interrupt options for different operational conditions
- ADC
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - ADC conversion time: 1.0 µs for 12-bit resolution (1 MHz), 0.88 µs conversion time for 10 bit resolution, faster conversion times can be obtained by lowering resolution.
  - Programmable sampling time
  - DMA support
- DAC
  - Left or right data alignment
  - DMA capability
  - External triggers for conversion
  - Programmable internal buffer
  - Input voltage reference, VDDA
  - FIFO Based operation

- TRNG(random number generator)
  - Max Rate: 20Mbps
- PMU_RTC
  - Internal 32KHz oscillator
  - Load time data to and read time data from seconds, minutes, hours and days counters
  - Support alarm settings
  - Interrupt sources:second, minute, hour,day interrupts,programmable alarm interrupts ,1KHZ/32KHZ periodic interrupts .
- Flexible Memory Controller(FMC)
  - Support SDR-SDRAM,up to sixteen row address bits, fifteen column address bits, and four bank address bits.
  - Support PSRAM up to 16Mbyte(support quad spi interface)
- PXLP
  - Single AHB master bus architecture
  - User programmable offset for sources and destination areas of picture for dma
  - User programmable sources and destination addresses on the whole memory space
  - Copy from an area to another
  - Support average filter algorithm
  - Support histogram algorithm
  - Support hough algorithm
  - Support Reed-Solomon(RS) error correction algorithm
  - Support binary image

  - Support look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA),The image split number of blocks is no more than 32. Support user programmable the block size.
  - Look for Minmum value,Maxmum value and computing average value in the block(Min_MAX_Average, MMA), support the image data from Digital Camera Interface (DCMI) directly.
  - Support black white run length coding algorithm
  - Interrupt generation on process completion
  - Support YOLO v3 deep learning end-to-end real-time target detection algorithm
  - Darknet light open source deep learning framework realized by YOLO v3, with less dependence and good portability. Due to its outstanding ability of speed and precision, especially small object detection, Darknet is widely used at present
- MIPI
  - The MIPI CSI-2 Host Controller supports the following features:
  - Compliant with MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2),Version 1.00 - 29 November 2005
  - Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
  - Supports up to 4 D-PHY Rx Data Lanes
  - Dynamically configurable multi-lane merging
  - Long and Short packet decoding
  - Timing accurate signaling of Frame and Line synchronization packets
  - Support for several frame formats such as:
  - General Frame or Digital Interlaced Video with or without accurate sync timing
  - Data type (Packet or Frame level) and Virtual Channel interleaving
  - 32-bit Image Data Interface delivering data formatted as recommended in CSI-2 Specification;
  - Supports all primary and secondary data formats:
  - RGB, YUV and RAW color space definitions
  - From 24-bit down to 6-bit per pixel

  - Generic or user-defined byte-based data types
  - Error detection and correction:
  - PHY level
  - Packet level
  - Line level
  - Frame level
- LCDC
  - compliance to the *AMBA Specification (Rev 2.0)* onwards foreasy integration into SoC implementation
  - dual 16-deep programmable 32-bit wide FIFOs for buffering incoming display
  - data
  - supports single and dual panel mono *Super Twisted Nematic* (STN) displays with 4 or 8-bit interfaces
  - supports single and dual-panel color and monochrome STN displays
  - supports *Thin Film Transistor (*TFT) color displays
  - resolution programmable up to 1024 x 768
  - 15 gray-level mono, 3375 color STN, and 32K color TFT support
  - 1, 2, or 4 *bits-per-pixel* (bpp) palettized displays for mono STN
  - 1, 2, 4 or 8 bpp palettized color displays for color STN and TFT
  - 16 *bits-per-pixel* (bpp) true-color non-palettized, for color STN and TFT
  - programmable timing for different display panels
  - 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically
  - frame, line and pixel clock signals
  - AC bias signal for STN and data enable signal for TFT panels
  - patented gray scale algorithm
  - supports little and big-endian, as well as WinCE data formats.
  - supports gamma correction
  - supports rgb565 output
- DCMI
  - 8-bit parallel interface(DVP)

  - Embedded/external line and frame synchronization
  - Continuous or snapshot mode
  - Crop feature
  - Supports the following data formats:
  - 8- bit progressive video: either monochrome or raw bayer
  - YCbCr 4:2:2 progressive video and gray output
  - YCbCr 4:2:0 directly output and gray output
  - RGB 565 progressive video and gray output
  - Compressed data: JPEG
  - Supports internal DMA and external DMA for RGB and gray data output simultaneously
  - Supports internal DMA and external DMA exchangable
  - Supports MIPI-IPI format
  - Supports Crop for gray window
- TSI
  - Support 16 channel input
  - Support trig mode and scan mode
  - Support lowpower mode and wakeup
- SSI
  - Serial-master operation
  - DMA controller interface – Enables the SSI to interface to a DMA controller over the bus using handshaking interface for transfer requests.
  - Clock stretching support in enhanced SPI transfers
  - Data item size (4 to 32 bits) – Item size of each data transfer under control of the programmer
  - FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 2 to 256 words deep. The FIFO width is fixed at 32 bits
  - Enhanced SPI support
  - Execute in Place (XIP) mode support
- GPIO
  - Support 136 GPIO

1.3 Block Diagram

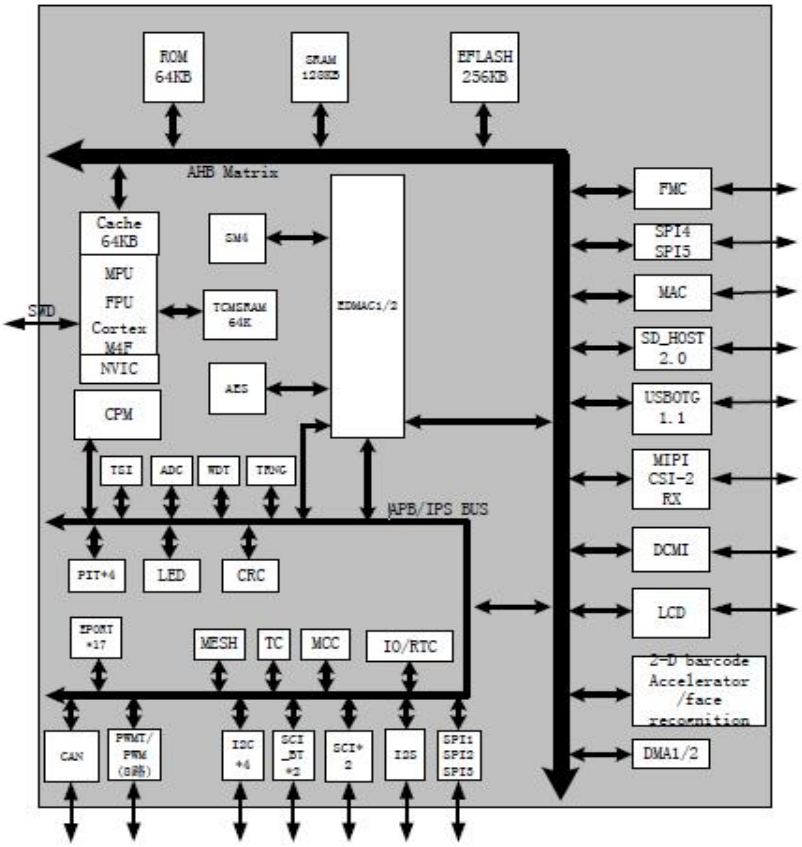

Figure 1-1 block diagram

Section 2 System Memory Map

2.1 Introduction

The address map, shown in **2.2**, includes:

- 64K Bytes of internal read only memory (ROM)
- 128K Bytes of internal static random-access memory (SRAM)
- 64K Bytes TCMSRAM
- 256K Bytes EFLASH
- Internal memory mapped registers

2.2 Address Map

Table 2-1 Boot Modes

mode[1]	mode[0]	Boot mode	Aliasing
0	0	ROM	ROM is selected as the boot space
0	1	EFLASH	EFLASH is selected as the boot space
1	0	SDRAM	SDRAM is selected as the boot space
1	1	SPI FLASH	SPI FLASH is selected as the boot space

Table 2-2 Memory mapping vs Boot mode/physical remap

Address	Boot/Remap in ROM	Boot/Remap in EFLASH	Boot/Remap in SDRAM	Boot/Remap in SPI FLASH
0xA4000000~ 0xA7FFFFFF	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD	SDRAM2LCD
0x80000000~ 0x87FFFFFF	SDRAM	SDRAM	SDRAM	SDRAM
0x20000000~ 0x2001FFFF	SRAM	SRAM	SRAM	SRAM
0x1FFF0000~ 0x1FFFFFFF	TCMSRAM	TCMSRAM	TCMSRAM	TCMSRAM
0x18000000~ 0x1BFFFFFF	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)	SDRAM (Cached)
0x14000000~ 0x17FFFFFF	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)	SPI2 FLASH (Cached)

Table 2-2 Memory mapping vs Boot mode/physical remap

0x10000000~ 0x13FFFFFF	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)	SPI1 FLASH (Cached)
0x08000000~ 0x0803FFFF	EFLASH	EFLASH	EFLASH	EFLASH
0x04000000~ 0x0400FFFF	ROM	ROM	ROM	ROM
0x00000000~ 0x03FFFFFF	ROM(64K) Aliased	EFLASH(256K) Aliased	SDRAM(16M) Aliased	SPI4(64M) Aliased

Table 2-3 Register Address Location Map

0x4000_0000	4Kbyte	AHB_IPS1	IO Control Module(IOCTRL)
0x4000_1000	4Kbyte		Chip configuration (CCM)
0x4000_2000	4Kbyte		Reset (RESET)
0x4000_3000	4Kbyte		TFM
0x4000_4000	4Kbyte		CPM
0x4000_5000	4Kbyte		Watchdog timer (WDT)
0x4000_6000	4Kbyte		TC
0x4000_7000	4Kbyte		PIT1
0x4000_8000	4Kbyte		PIT2
0x4000_9000	4Kbyte		Edge Port 16(EPORT16)
0x4000_a000	4Kbyte		EDMAC1
0x4000_b000	4Kbyte		Edge Port 14(EPORT14)
0x4000_c000	4Kbyte		Edge Port 15(EPORT15)
0x4000_d000	4Kbyte		PIT3
0x4000_e000	4Kbyte		PIT4
0x4000_f000	4Kbyte		CAN
0x4001_0000	4Kbyte		SPI1
0x4001_1000	4Kbyte		SPI2
0x4001_2000	4Kbyte		SPI3
0x4001_3000	4Kbyte		SCI_BT1
0x4001_4000	4Kbyte		SCI_BT2
0x4001_5000	4Kbyte		Reserved
0x4001_7000	4Kbyte		I2C
0x4001_8000	4Kbyte		PWM
0x4001_9000	4Kbyte		Edge Port (EPORT)
0x4001_a000	4Kbyte		Edge Port 1(EPORT1)
0x4001_b000	4Kbyte		I2C2
0x4001_c000	4Kbyte		I2C3
0x4001_d000	4Kbyte		SCI1

0x4001_e000	4Kbyte	AHB_IPS1	SCI2
0x4001_f000	4Kbyte		PWMT
0x4002_0000	4Kbyte		ADC
0x4002_1000	4Kbyte		DAC
0x4002_3000	4Kbyte		TSI
0x4002_4000	4Kbyte		Edge Port 2(EPORT2)
0x4002_5000	4Kbyte		Edge Port 3(EPORT3)
0x4002_6000	4Kbyte		Edge Port 4(EPORT4)
0x4002_7000	4Kbyte		Edge Port 5(EPORT5)
0x4002_8000	4Kbyte		Edge Port 6(EPORT6)
0x4002_9000	4Kbyte		Edge Port 7(EPORT7)
0x4002_a000	4Kbyte		Edge Port 8(EPORT8)
0x4002_b000	4Kbyte		Edge Port 9(EPORT9)
0x4002_c000	4Kbyte		Edge Port 10(EPORT10)
0x4002_d000	4Kbyte		Edge Port 11(EPORT11)
0x4002_e000	4Kbyte		Edge Port 12(EPORT12)
0x4002_f000	4Kbyte		Edge Port 13(EPORT13)
0x4003_1000	4Kbyte		True Random Number Generator (TRNG)
0x4003_5000	4Kbyte		PMU_RTC
0x4003_6000	4Kbyte	AHB_IPS2	Reserved
0x4003_7000	4Kbyte		CRYPTO
0x4003_8000	4Kbyte		SHA
0x4003_9000	4Kbyte		EDMAC0
0x4003_a000	4Kbyte		Reserved
0x4004_4000	4Kbyte	AHB2	CRC0
0x4004_5000	4Kbyte		CRC1
0x4004_6000	4Kbyte		DMAC1
0x4004_7000	4Kbyte		DMAC2
0x4004_8000	4Kbyte		CLCD
0x4004_9000	4Kbyte		TRNG_OSC
0x4004_a000	4Kbyte		SD_HOST

0x4004_c000	4Kbyte	AHB3	USBC
0x4005_0000	4Kbyte	AHB_APB	MIPI
0x4005_1000	4Kbyte		Cache_Config
0x4005_2000	4Kbyte		DMA2D
0x4005_3000	4Kbyte		DCMI
0x4005_4000	4Kbyte		PXLP
0x4005_5000	4Kbyte		Cache2_Config
0x4005_6000	4Kbyte		DCMI_DVP
0x4005_7000	4Kbyte		I2S
0x4006_0000	64Kbyte	AHB_MAC	MAC
0x6000_0000	4Kbyte	AHB_SPI4	SPI4
0x7000_0000	4Kbyte	AHB_SPI5	SPI5
0x9c00_0000	4Kbyte	AHB_SDRAM	SDRAM
0xa800_0000	4Kbyte	AHB_SDRAM2LCD	SDRAM2LCD
0xe000_0000	4Kbyte	M4	M4 SYS

System Memory Map

Section 3 Signal Description

3.1 Introduction

The chip is available in package:

- BGA169 (including 8MB SDRAM and 2MB SPIFLASH)

3.2 Package Pinout Summary

Refer to :

Table 3-1 for 169-pin BGA package

Table 3-1 BGA 169 package

MIPIPHY_AVDD	VIN1	VCM1	ADC_IN[2]	ADC_IN[0]	ADC_IN[4]	DAC_OUT	SCK1	SS1	DM	POR	VDD	USBDET
MIPI_DATAP[0]	VIN2	VCM2	ADC_IN[5]	ADC_IN[3]	ADC_IN[1]	MOSI1	MISO1	WAKEUP	DP	SDIO[5]	SDIO[6]	PAD_AVDD_BBAT
MIPI_DATAN[0]	VIN3	VDD33	RSTOUT	AVDD_MCC_ADC	AVDD_DAC	VDD_PD	ISODAT3	ISORST3	OTG_ID	SDIO[7]	SDIO[4]	PAD_XTALO
MIPI_CLKN	MIPI_CLKP	VCM3	VDD33	VDD33	VDDA	VDD18	VDDIO_CARD1	ISOCLK3	OTG_VBUS	SDIO[2]	SDIO[3]	PAD_XTALI
TXD4	RXD4	VSS	VDD33	VDD33	AVSS_MCC_ADC	VSS	VCC5V	VDD33	SDIO[1]	SDIO[0]	RXD2	TXD2
TXD3	RXD3	VSS	VSS	VSS	VDD33_FMC_DATA	VSS	VSS	VDD33	AVDD_TSI	SCL	SDA	GINT[0]
XTAL	EXTAL	DCMI_DATA[7]	DCMI_DATA[5]	DCMI_VSYNC	VDD33_FMC_DATA	VDD33_FMC_DATA	VSS	CLKOUT	GINT[6]	GINT[2]	GINT[4]	GINT[1]
GINT[14]	GINT[15]	DCMI_DATA[6]	DCMI_DATA[1]	DCMI_DATA[4]	DCMI_HSYNC	VDD33	VSS	GINT[5]	GINT[3]	GINT[7]	SDH_DAT[3]	SDH_CLK
DCMI_DATA[3]	DCMI_DATA[2]	DCMI_PCLK	SENSOR_CLKIN	DCMI_DATA[0]	VSS	VDD33_FMC_DATA	VSS	VDD33	VSS	VSS	SDH_DAT[2]	SDH_CARDINT
VDD33_FMC_DATA	SCL3	SDA3	LCD_CLD[5]	VSS	VSS	VSS	VDD33	VSS	VSS	MISO2	SDH_DAT[0]	SDH_WPRT
MODE[1]	MODE[0]	LCD_CLD[6]	LCD_CLD[4]	VSS	LCD_CLD[9]	LCD_CLD[2]	VDD33	VSS	VSS	SS2	SCK2	SDH_CMD
LCD_CLD[3]	LCD_CLD[11]	LCD_CLD[12]	LCD_CLD[15]	LCD_CLD[14]	LCD_CLLP	LCD_CLD[0]	VSS	VSS	VSS	VSS	MOSI2	SDH_DAT[1]
LCD_CLD[10]	LCD_CLD[7]	LCD_CLCP	LCD_CLAC	LCD_CLD[13]	LCD_CLFP	LCD_CLD[8]	LCD_CLD[1]	VSS	VDD33	VDD33	VSS	SDH_DET

3.3 Signal Properties Summary

below is the signal description.

Table 3-2 Signal Description

PIN No.	PIN Name	ALT1	ALT2	ALT3	comment
A1	MIPIPHY_AVDD				
A2	VIN1				
A3	VCM1				
A4	ADC_IN[2]				
A5	ADC_IN[0]				
A6	ADC_IN[4]				
A7	DAC_OUT				
A8	SCK1	pwm[5]	gint[8]	i2c3_filter[1]	
A9	SS1	pwm[4]	gint[10]	i2c3_filter[0]	
A10	DM				
A11	POR				
A12	VDD				
A13	USBDET				
B1	MIPI_DATAP[0]				
B2	VIN2				
B3	VCM2				
B4	ADC_IN[5]				
B5	ADC_IN[3]				
B6	ADC_IN[1]				
B7	MOSI1	pwm[6]	gint[9]	i2c3_filter[3]	
B8	MISO1	pwm[7]	gint[11]	i2c3_filter[2]	
B9	WAKEUP				
B10	DP				
B11	SDIO[5]				
B12	SDIO[6]				
B13	PAD_AVDD_BBAT				
C1	MIPI_DATAN[0]				
C2	VIN3				
C3	VDD33				

Table 3-2 Signal Description

PIN No.	PIN Name	ALT1	ALT2	ALT3	comment
C4	RSTOUT	GPIO			
C5	AVDD_MCC_ADC				
C6	AVDD_DAC				
C7	VDD_PD				
C8	ISODAT3		gint[117]		
C9	ISORST3		gint[118]		
C10	OTG_ID				
C11	SDIO[7]				
C12	SDIO[4]				
C13	PAD_XTALO				
D1	MIPI_CLKN				
D2	MIPI_CLKP				
D3	VCM3				
D4	VDD33				
D5	VDD33				
D6	VDDA				
D7	VDD18				
D8	VDDIO_CARD1				
D9	ISOCLK3		gint[116]		
D10	OTG_VBUS				
D11	SDIO[2]				
D12	SDIO[3]				
D13	PAD_XTAL				
E1	TXD4	can_tx	gint[84]		
E2	RXD4	can_rx	gint[85]		
E3	VSS				
E4	VDD33				
E5	VDD33				
E6	AVSS_MCC_ADC				
E7	VSS				
E8	VCC5V				
E9	VDD33				
E10	SDIO[1]				
E11	SDIO[0]				
E12	RXD2	pwm_timer_N[1]	gint[17]	tsi_ch[2]	
E13	TXD2	pwm_timer_N[0]	gint[16]	tsi_ch[3]	
F1	TXD3	pwm_timer_N[2]	gint[82]	ipp_do_mtm_rtc[16]	

Table 3-2 Signal Description

PIN No.	PIN Name	ALT1	ALT2	ALT3	comment
F2	RXD3	pwm_timer_N[3]	gint[83]	ipp_do_mtm_rtc[17]	
F3	VSS				
F4	VSS				
F5	VSS				
F6	VDD33_FMC_DATA				
F7	VSS				
F8	VSS				
F9	VDD33				
F10	AVDD_TSI				
F11	SCL	tsi_ch[0]	gint[18]	chip_test_tdi	
F12	SDA	tsi_ch[1]	gint[19]		
F13	GINT[0]	tsi_ch[4]	sd_i2s	ipp_do_mtm_rtc[8]	
G1	XTAL				
G2	EXTAL				
G3	DCMI_DATA[7]	miso3	gint[111]	mbt_out[7]	
G4	DCMI_DATA[5]	sck3	gint[109]	mbt_out[5]	
G5	DCMI_VSYNC		gint[114]		
G6	VDD33_FMC_DATA				
G7	VDD33_FMC_DATA				
G8	VSS				
G9	CLKOUT				
G10	GINT[6]	tsi_ch[10]	sci4_rts	ipp_do_mtm_rtc[14]	
G11	GINT[2]	tsi_ch[6]	sclk_i2s	ipp_do_mtm_rtc[10]	
G12	GINT[4]	tsi_ch[8]	mclk_i2s	ipp_do_mtm_rtc[12]	
G13	GINT[1]	tsi_ch[5]	lrck_i2s	ipp_do_mtm_rtc[9]	
H1	GINT[14]	tio/tms	pwm[2]		
H2	GINT[15]	tclk	pwm[3]		
H3	DCMI_DATA[6]	mosi3	gint[110]	mbt_out[6]	
H4	DCMI_DATA[1]	sck2	gint[105]	mbt_out[1]	
H5	DCMI_DATA[4]	ss3	gint[108]	mbt_out[4]	
H6	DCMI_HSYNC		gint[112]		
H7	VDD33				
H8	VSS				
H9	GINT[5]	tsi_ch[9]		ipp_do_mtm_rtc[13]	

Table 3-2 Signal Description

PIN No.	PIN Name	ALT1	ALT2	ALT3	comment
H10	GINT[3]	tsi_ch[7]	nreset_i2s	ipp_do_mtm_rtc[11]	
H11	GINT[7]	tsi_ch[11]	sci4_cts	ipp_do_mtm_rtc[15]	
H12	SDH_DAT[3]	phy_rxd[1]	gint[134]		
H13	SDH_CLK	rmii_clk	gint[119]		
J1	DCMI_DATA[3]	miso2	gint[107]	mbt_out[3]	
J2	DCMI_DATA[2]	mosi2	gint[106]	mbt_out[2]	
J3	DCMI_PCLK	bist1_clk	gint[113]		
J4	SENSOR_CLKIN		gint[115]		
J5	DCMI_DATA[0]	ss2	gint[104]	mbt_out[0]	
J6	VSS				
J7	VDD33_FMC_DATA				
J8	VSS				
J9	VDD33				
J10	VSS				
J11	VSS				
J12	SDH_DAT[2]	phy_rxd[0]	gint[133]		
J13	SDH_CARDINT	phy_rxdv	gint[135]		
K1	VDD33_FMC_DATA				
K2	SCL3				
K3	SDA3				
K4	LCD_CLD[5]	sdram2lcd[5]	gint[125]	fls_ctrl_pin2pad[5]	
K5	VSS				
K6	VSS				
K7	VSS				
K8	VDD33				
K9	VSS				
K10	VSS				
K11	MISO2	pwm_timer[3]	gint[74]	sdr_bank_addr[0]	
K12	SDH_DAT[0]	phy_txd[0]	gint[131]		
K13	SDH_WPRT	phy_txen	gint[130]		
L1	MODE[1]	GPIO			
L2	MODE[0]	GPIO			
L3	LCD_CLD[6]	sdram2lcd[6]	gint[126]	fls_ctrl_pin2pad[5]	
L4	LCD_CLD[4]	sdram2lcd[4]	gint[124]	fls_ctrl_pin2pad[4]	
L5	VSS				
L6	LCD_CLD[9]	sdram2lcd[9]	gint[25]	ITR3	

Table 3-2 Signal Description

PIN No.	PIN Name	ALT1	ALT2	ALT3	comment
L7	LCD_CLD[2]	sdram2lcd[2]	gint[122]	fls_ctrl_pin2pad[2]	
L8	VDD33				
L9	VSS				
L10	VSS				
L11	SS2	pwm_timer[0]	gint[72]	sdr_cas_n	
L12	SCK2	pwm_timer[1]	gint[73]	sdr_ras_n	
L13	SDH_CMD	rmii_mdc	gint[128]		
M1	LCD_CLD[3]	sdram2lcd[3]	gint[123]	fls_ctrl_pin2pad[3]	
M2	LCD_CLD[11]	sdram2lcd[11]	gint[27]		
M3	LCD_CLD[12]	sdram2lcd[12]	gint[28]		
M4	LCD_CLD[15]	sdram2lcd[15]	gint[31]		
M5	LCD_CLD[14]	sdram2lcd[14]	gint[30]		
M6	LCD_CLLP	sdram2lcd_we_n	gint[103]		
M7	LCD_CLD[0]	sdram2lcd[0]	gint[120]	fls_ctrl_pin2pad[0]	
M8	VSS				
M9	VSS				
M10	VSS				
M11	VSS				
M12	MOSI2	pwm_timer[2]	gint[75]	sdr_bank_addr[1]	
M13	SDH_DAT[1]	phy_txd[1]	gint[132]		
N1	LCD_CLD[10]	sdram2lcd[10]	gint[26]		
N2	LCD_CLD[7]	sdram2lcd[7]	gint[127]		
N3	LCD_CLCP	sdram2lcd_oe_n	gint[95]		
N4	LCD_CLAC	sdram2lcd_addr	gint[94]		
N5	LCD_CLD[13]	sdram2lcd[13]	gint[29]		
N6	LCD_CLFP	sdram2lcd_cs_n	gint[102]		
N7	LCD_CLD[8]	sdram2lcd[8]	gint[24]	ITR2	
N8	LCD_CLD[1]	sdram2lcd[1]	gint[121]	fls_ctrl_pin2pad[1]	
N9	VSS				
N10	VDD33				
N11	VDD33				
N12	VSS				
N13	SDH_DET	rmii_mdio	gint[129]		

Signal Description

Section 4 Package information

4.1 General

This section provides parameters for below items:

• Package Outline Dimension (POD) of package for BGA169

4.2 POD of Package BGA169

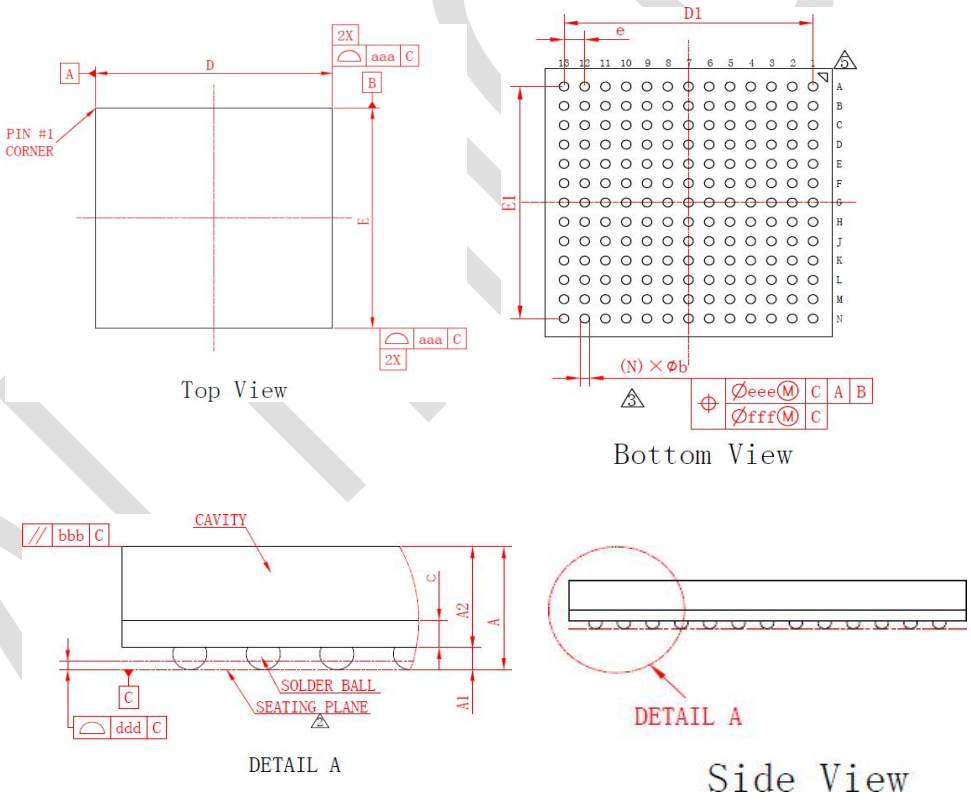

Figure 4-1 POD of Package BGA169

Table 4-1 POD Parameters of package BGA169

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.270	---	---	0.050
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
c	0.230	0.260	0.290	0.009	0.010	0.011
D	8.900	9.000	9.100	0.350	0.354	0.358
E	8.900	9.000	9.100	0.350	0.354	0.358
D1	---	7.800	---	---	0.307	---
E1	---	7.800	---	---	0.307	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball diam	0.300			0.012		
N	169			169		
MD/ME	13/13			13/13		

Appendix A Preliminary Electrical Characteristic

A.1 General

This section provides electrical parametrics and electrical ratings for the microcontroller unit.

A.2 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the Chip can be exposed without permanently damaging it. See **Table A-1**.

The Chip contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table. Connect unused inputs to the appropriate voltage level, V_{DDH}. This device is not guaranteed to operate properly at the maximum ratings. Refer to **A.4**, **A.4**,**Table A-3**,**Table A-4** for guaranteed operating conditions.

Table A-1 Absolute Maximum Ratings

Num	Rating	Symbol	Value	Unit
1	Operating temperature range	T_{OPT}	-25 to +85	^{O}C
2	Storage temperature range	T_{STG}	-40 to +125	^{O}C

A.3 Electrostatic Discharge (ESD) Protection

Table A-2 ESD Protection Characteristics

Parameter[1,2,3,4,5]	Symbol	Value	Units
ESD target for human body model	HBM	2000	V
Latch Up	Latch UP	200	mA

NOTES:

1. This report will be invalid if reproduced in whole or in part.
2. This report refers only to the specimen(s) submitted to test, and is invalid if used separately.
3. This report is ONLY valid with the examination seal and signature of this institute.
4. The tested specimen(s) will only be preserved for thirty days from the date issued, if not collected by the applicant.
5. The failure criteria of all ESD tests should be based on the result of parametric and functional testing conducted by the customer, which follows the statement of international standards. Thus, the judgment of the curve traces provided in this report is for reference ONLY.

A.4 DC Electrical Specifications

Table A-3 DC Electrical Specificatios(3.3V)

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{DDH}	3	3.3	3.6	V
Input High Voltage	V_{IH}	2	—	DVDD	V
Input Low Voltage	V_{IL}	VSS	—	0.8	V
Output High Voltage	V_{OH}	2.4	—	DVDD	V
Output Low Voltage	V_{OL}	VSS	—	0.4	V
Pull-up Resistor current	R_{PU}	50	—	—	υA
Input Leakage Current@DVDD=max,VPAD-0 o DVDD	I_{IN}	-1.2	—	1.2	υA
Fail leakagecurrent @DVDD=0,VPAD=DVDD=max	I_{PAD}	—	—	1.2	υA
Off_state leakage current@DVDD=max,VPAD=0 or DVDD	I_{OZ}	—	—	1.2	uA

A.5 Power Consumption

Table A-4 power consumption[1]

Parameter	power consumption	
	400MHz	**500MHz**
CPU run	80mA	120mA
CPU and peripherals run[1]	130mA	170mA
CPU and SDRAM run[2]	97mA	136mA
CPU,SDRAM and peripherals run	134mA	180mA
LOWPOWER MODE[3]	5mA	
POWEROFF1.0 MODE[4]	10uA	
POWEROFF2.0 MODE[5]	180nA	

NOTES:

1. All the peripherals are operated in fastest speed.
2. CPU:SDRAM=4:1 in speed.
3. Chip poweron and clock stop.

wakeup source: USI,I2C,EPORT,USB RESUME,TSI TOUCH,TIME COUNTER, RTC,WK PAD,USBDET,POR,PCI

4. Only TSI run in poweroff 1.0 mode.

wakeup source: EPORT0,TSI TOUCH,RTC,WK PAD,USBDET,POR,PCI

5. Only PCI poweron.

wakeup source: WK PAD,USBDET,POR

NOTES:

1. All the data are typical results.

A.6 AC Timing

A.6.1 SPI Interface

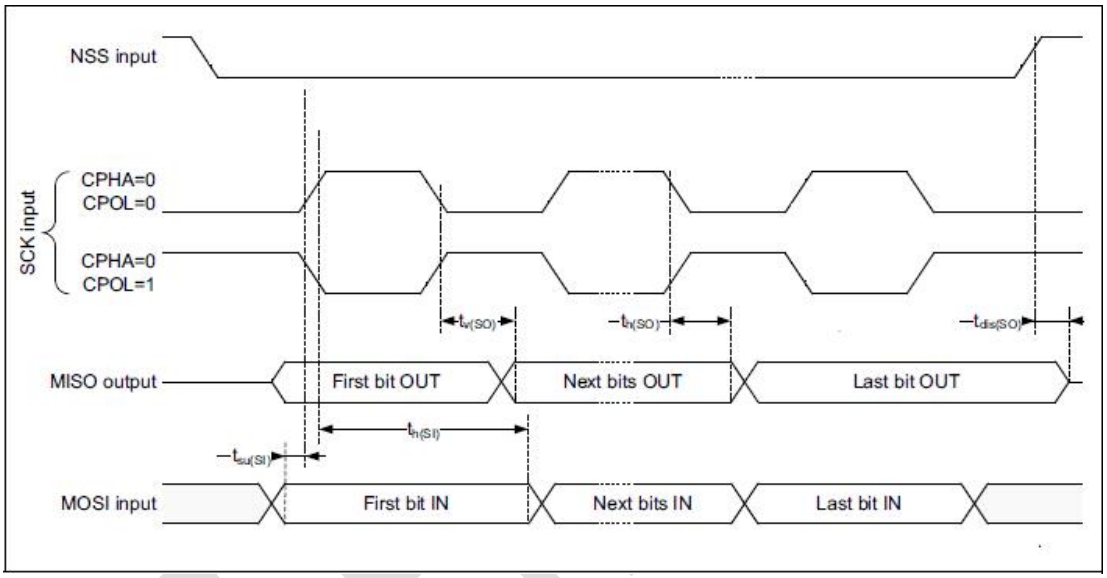

Figure A-1 SPI timing diagram

Table A-5 SPI characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SPI clock frequency	VCC3.3V,VDD 1.1V	-	-	50	MHz
		VCC3.3V,VDD 1.23V	-	-	62.5	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	-	3.9	6.9	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	-1	0	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	5.9	8	11.9	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	9.8	14.95	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	2.3	3.9	-	

A.6.2 SSI(QSPI) Interface

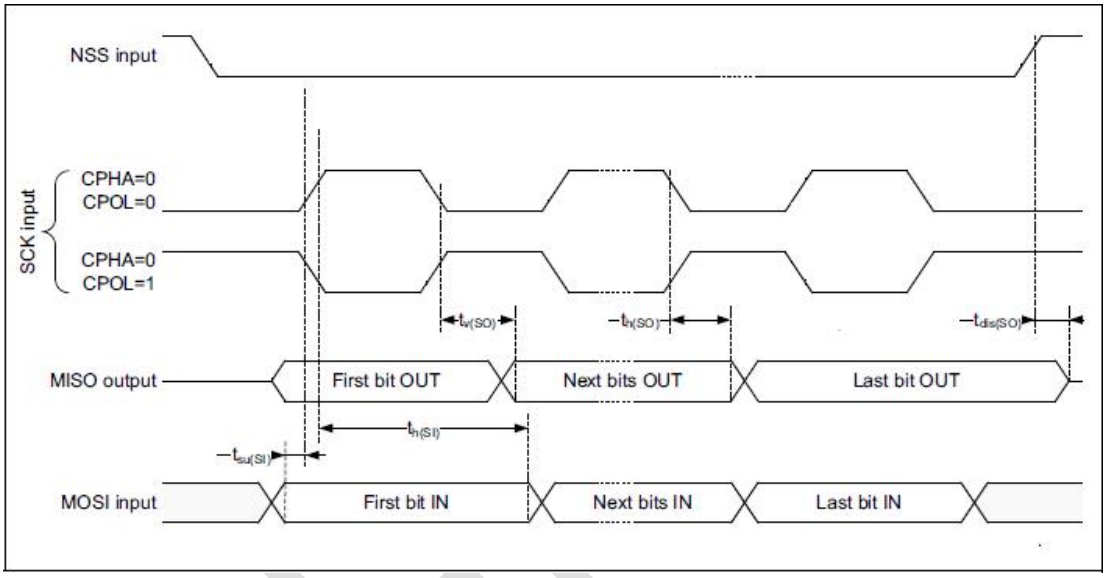

Figure A-2 SSI(QSPI) timing diagram

Table A-6 SSI(QSPI) characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SSI clock frequency	VCC3.3V,VDD 1.1V	-	-	100	MHz
		VCC3.3V,VDD 1.23V	-	-	125	
$t_{su(SI)}$	Data input setup time	VCC3.3V,VDD1.1V	2	-	-	ns
$t_{h(SI)}$	Data input hold time	VCC3.3V,VDD1.1V	3	-	-	
$t_{dis(SO)}$	Data output disable time	VCC3.3V,VDD1.1V	-	-	7	
$t_{v(SO)}$	Data output valid time	VCC3.3V,VDD1.1V	-	-	6	
$t_{h(SO)}$	Data output hold time	VCC3.3V,VDD1.1V	0	-	-	

A.6.3 SDRAM Interface

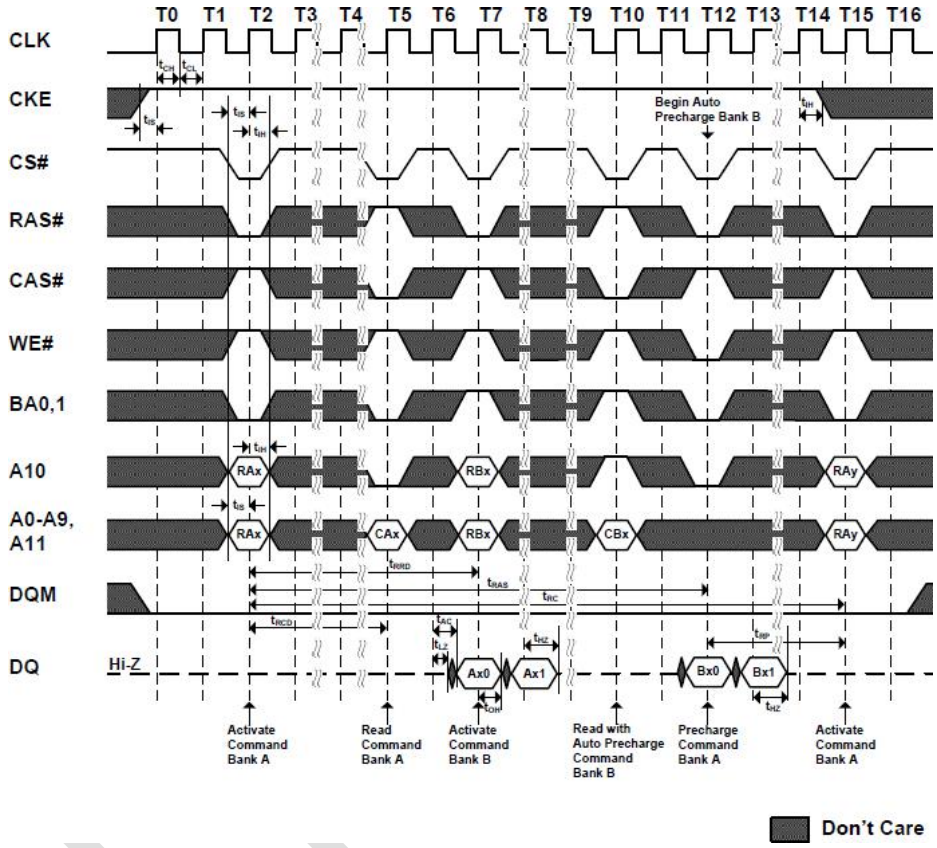

Figure A-3 Read Timing diagram (Burst Length =2,CAS# Latency=2)

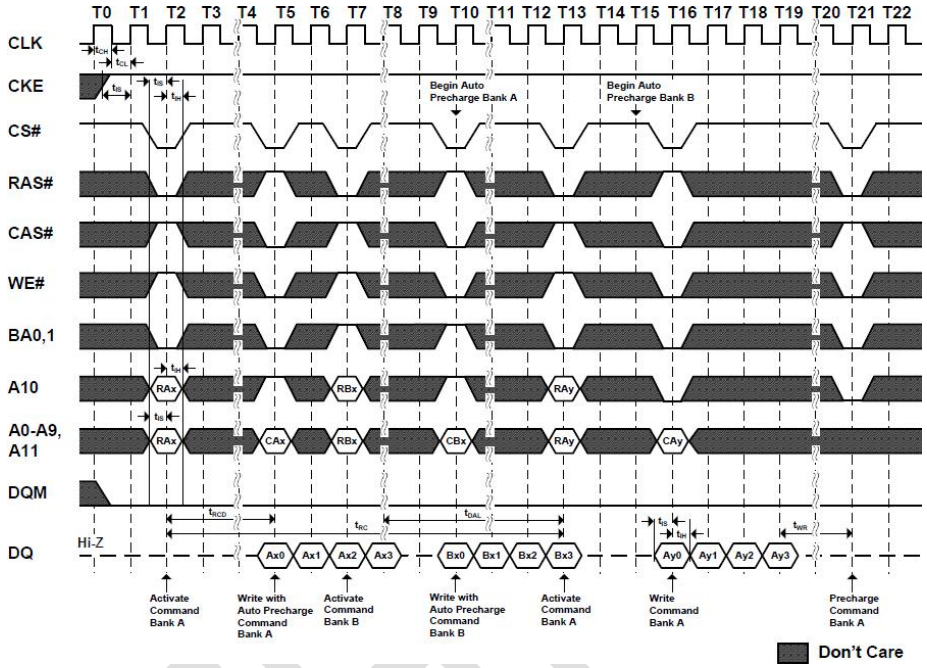

Figure A-4 Write Timing diagram (Burst Length =4)

Table A-7 SDRAM characteristics

Symbol	Parameter	condition	min	typ	max	Unit
f_{sck}	SDRAM clock frequency	VCC3.3V,VDD 1.1V	-	-	100	MHz
		VCC3.3V,VDD 1.23V	-	-	125	
t_{IS}	Data/Address/Control input setup time	VCC3.3V,VDD1.1V	1.5	-	-	ns
t_{Ih}	Data/Address/Control input hold time	VCC3.3V,VDD1.1V	0.8	-	-	
t_{OH}	Data output hold time	VCC3.3V,VDD1.1V	0	-	-	